A Highly Integrated 65-nm SoC Process with Enhanced Power/Performance of Digital and Analog Circuits


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Abstract

65nm Deeply Depleted Channel (DDC™) transistors have been fabricated with a halo-free, un-doped epitaxial channel and enable reduced threshold voltage ($V_T$) variation, lower supply voltage ($V_{CC}$), enhanced body effect and $I_{EFF}$. Digital circuits made using this technology show benefits ranging from 47% power reduction to 38% frequency increase. Analog circuits exhibit 4x greater amplifier gain despite lower $V_{DD}$, and current mirror mismatch (both global and local) shows 40% and 30% reduction for NMOS and PMOS, respectively.

Introduction

There is great incentive to enhance the power/performance of fully amortized technologies, i.e., at 40-nm and larger lithography, that are cost-effective and widely used in consumer mobile products. We have previously disclosed a low variation, undoped channel, planar transistor at 65-nm with dramatically improved $V_T$ matching and subsequent reduction in SRAM array leakage and minimum operating voltage ($V_{min}$) [1]. This paper presents logic and analog circuit-level improvements realized by further optimization of device parameters including global and local $V_T$ variation, junction leakage, body coefficient and $I_{EFF}$. Ring oscillator (RO) measurements demonstrate nearly 50% improvement in active power dissipation at matched frequency and 40% speed-up at matched $V_{DD}$. Systematic $V_T$ variability is reduced by one sigma. In addition, even tighter design corners can be achieved through appropriate body biasing. We also demonstrate integration of analog functionality at 300mV lower nominal $V_{DD}$. OTA circuits average 4x gain improvement and 30% lower worst-case measured offset voltage. Current mirrors exhibit improvements in both global and local mismatch, greater than 40% and 30% for NMOS and PMOS, respectively. VCO power is reduced and effective frequency range is increased over 2x, allowing a fully-integrated ultra-low power 65nm platform.

Process Integration

The device fabrication flow and structure used in this work are outlined in Fig. 1. Well, screen, and $V_T$ setting layers are formed first, followed by a blanket undoped epitaxial (epi) layer deposition. Then, STI is formed, followed by high voltage I/O wells, logic and I/O oxide, poly gate, LDD, and source/drain (S/D) implant. Epi thickness is an important parameter determining $V_T$ as it directly relates to depletion depth $W_{dep}$. As such, it can be an effective dial for $V_T$ control. A tight epi processing window ensures manufacturability.

Device and Circuit Impact

The new device structure improves a number of transistor parameters that enhance circuit performance, including random and systematic (corner) variation control and speed/power performance. Transistor variation is dramatically improved by the undoped channel and the highly doped screening layer, which reduces RDF and depletion depth ($W_{dep}$) variation. This, in turn, improves both global and local $V_T$ variation (Fig. 3). Global $V_T$ variation is improved by 1σ and SRAM mismatch is improved by 40% and 60% for PMOS and NMOS, respectively. For SRAM NMOS devices, extremely low mismatch (sub-15mV) is repeatedly demonstrated. Fig. 4 shows measurements of transistor arrays at standard cell pitch, having different length of diffusion (LOD). $V_T$ variations caused by scattered well implant dopants are kept away from the channel by the subsequent undoped epi layer deposition validating that well proximity effects are mitigated. Therefore, elimination of halo implants removes $V_T$ variation components due to those proximity effects.

The independent $V_T$ setting layer allows a wide threshold voltage range with minimal increase in $V_T$ variation and junction leakage. The technology thus supports the wide device leakage/performance range required for mobile system on chip designs. Fig. 5 demonstrates this by SRAM mismatch that is almost constant across a $V_T$ range of ~200mV for PMOS and ~80mV for NMOS. Fig 6 shows junction leakage is independent of $V_T$ (data points are...
representative of individual wafers with various process conditions and applied reverse body biases range from 0 to 0.6V in magnitude).

The screening layer that is a critical component of the well profile not only determines the channel depletion depth but also produces a high body coefficient (BC) of 240mV/V. Fig. 7 shows the body bias response of transistors fabricated at SS, TT, and FF process corner conditions. The improved body control allows a wide range of performance as well as circuit level variability mitigation [2]. The FF and SS distributions at the nominal back bias of 0.3V on the universal curve (Fig. 7a and Fig. 7c for NMOS and PMOS, respectively) are pulled substantially towards the TT behaviors using 0V back bias for SS and 0.6V back bias for FF (Fig. 7b and Fig. 7d). Fig. 8 shows ID-VD behavior for both NMOS and PMOS control and DDC devices with V_DS = 0.6V, 0.9V and 1.2V in the geometry range typical for analog circuits. The DDC devices are body biased to match their Idsat to the control and DDC devices with V GS = 0.6V, 0.9V and 1.2V in the saturation region. Moreover, the undoped channel improves channel mobility. Unlike long L (Fig. 8), nominal channel length (logic) devices show similar PMOS and NMOS improvement. The better DIBL and mobility benefit of the DDC transistors with 20% to 80% higher I eff [3], in particular at low V DD, as Fig. 9 shows.

The transistor level improvements transfer to circuits in ways that benefit IC power/performance. Fig 10 shows the frequency versus power response for a halo control inverter RO at V DD = 1.2V and the same RO circuit using DDC device at V DD = 0.9V (both their nominal V DD). Each symbol represents a RO at one corner with reverse body bias applied from 0 to 0.8V. Overlap between the FF and SS device measurements further demonstrates the ability to pull in DDC circuit delay from the corner values. The better I eff, particularly at low V DS, mitigates the high BC impact on stacked gate delay, e.g., multi-input NAND and NOR gates have equal or better delay despite their higher BC (Fig. 11) as in [4]. Fig. 12 demonstrates RO response with various V DD and body bias applied (for clarity only TT is shown). A power benefit of 47% at matching RO frequency or a performance benefit (RO frequency increase) of 38% for the same total power dissipation is achieved across the supply voltage range. The control and DDC devices in Fig. 12 do not have matched I off—the latter have greater leakage, traded off against active power. A primarily digital block (4.1mm x 8.2mm) comprising a 5.85M gate coprocessor and 1.45Mb SRAM on the DDC transistors achieves 47% total power reduction with no layout changes at nominal V DD, i.e., 1.2V for control and 0.9V for DDC, running at the same frequency (Fig. 13). This design utilizes both high and low V T devices, and shows similar static and dynamic power improvement.

SOC designs require analog circuits on both the thick gate high voltage and thin gate core devices. The process flow described above enables on-chip integration of thin-oxide DDC devices and thick-oxide legacy (analog/IO) devices. Analog/IO parametrics are essentially unchanged, allowing existing IP blocks to be used without modification. Here, these transistors are fabricated conventionally, by implanting through the epitaxial layer after DDC core device fabrication as shown in Fig. 1. For analog circuits on thin gate core devices, as with digital circuits, the DDC transistors provide better matching, as well as up to 4x improved Rout.

Fig. 14 shows normalized frequency vs. power for a VCO measured with different bias currents. The DDC process shows over 2x greater frequency range and maximum frequency at the same power. An operational transconductance amplifier (OTA) fabricated on both the control and DDC transistors, provides further comparison. The circuits operate at their nominal V DD of 1.2V and 0.9V, respectively. Fig. 15a shows measured transfer curves of OTA on control and DDC process. Fig. 15b shows their gain comparison. The OTA fabricated with the DDC transistors shows ~12dB gain improvement despite its lower operating voltage. This gain improvement is due to the lower DIBL, which as mentioned, increases Rout. Another commonly used analog circuit is the current mirror, which here has a number of identical and multiplying outputs. Current matching is critical for many circuits operation. NMOS and PMOS current mirrors were fabricated on the DDC and control process for comparison. The nominal mirror supply current is 5µA, and 1x and multiplying (2x, 4x, 16x) output currents are measured separately, to evaluate local and global current mismatches. Fig. 16a and Fig. 16b compare both local and global current mismatch on the DDC and control process. For local current mismatch DDC process shows 40% and 30% reduction in NMOS and PMOS, respectively. For global current mismatch similar results are obtained (table 1). This matching improvement is attributed to the benefit of undoped epi channel and screen layer in DDC transistors, which results in lower RDF and W dep variation.

Conclusion

Circuit-level benefits realized via 65-nm DDC transistors with reduced V T variation, increased BC and I eff have been presented. Logic improvements range from approximately 50% power reduction to 40% frequency increase. Analog circuits benefit from lower voltage operation, greater amplifier gain, and improvement in both local and global matching.

References

Fig. 1. a) Process flow showing STI formation is after well implantation and channel formation and b) the resulting structure with an undoped channel.

Fig. 2. Epitaxial layer thickness uniformity at the wafer level. Wafer $\sigma = 0.25\%$; overall $1\sigma = 0.65\%$

Fig. 3. a) Global W/W variation of the control and DDC NMOS and PMOS $V_T$, b) SRAM transistor matching of the control and DDC pull-up (PU) PMOS, pull-down (PD) NMOS and pass-gate (PG) NMOS transistors, improved by 40%, 60%, and 60%, respectively.

Fig. 4. Transistor array results: $\sigma V_T$ of DDC and control logic transistors in standard logic layouts.

Fig. 5. $\sigma V_T$ of DDC SRAM transistor vs. the $V_T$ target. Unlike halo processes, the $\sigma V_T$ is essentially invariant over the $V_T$ range.

Fig. 6. Long channel transistor total leakage is used to evaluate junction leakage $I_J$, which dominates at long $L$. a) NMOS and b) PMOS leakage vs. target $V_T$. Low junction leakage is achieved and the choice of $V_T$ does not significantly impact $I_J$.

Fig. 7. The DDC transistor screening layer affords a strong body coefficient that allows effective use of body bias to mitigate systematic process corner variation. a) $I_{off}$ vs. $I_{on}$ NMOS at fast, typical and slow (F, T, S) corners with -0.3 $V_{SB}$ and b) $I_{off}$ vs. $I_{on}$ NMOS with -0.6 $V_{SB}$ on F, 0V $V_{SB}$ on S silicon effectively merges the corners. c) and d) demonstrate the same for DDC PMOS transistors.
Fig. 8. $I_{DS}-V_{DS}$ comparison between DDC and control devices for typical analog W/L = 5/0.5μm.

Fig. 9. Relative effective drive current of DDC NMOS and PMOS logic L vs. control. Low DIBL provides a large advantage at low $V_{DD}$.

Fig. 10. Measured RO power vs. frequency at multiple $V_{DD}$ and $V_{SS}$. Overlap between FF and SS demonstrates ability to pull in delay corners.

Fig. 11. Normalized measured NAND and NOR RO frequencies. High $I_{DS}$ at low $V_{DS}$ mitigates the high BC impact on stacked gates.

Fig. 12. Measured RO power vs. frequency demonstrating 38% improved performance at fixed $V_{DD}$ and 47% lower power at fixed frequency.

Fig. 13. Normalized power dissipation of an 4.1x8.2mm coprocessor test chip on the control and DDC process at their nominal $V_{DD}$ running at the same frequency.

Fig. 14. Normalized VCO frequency with different bias current on the DDC and control process demonstrating over 2x greater frequency range and top frequency.

Fig. 15. Operational transconductance amplifier transfer curves measured from circuits fabricated on the control and improved transistor processes at their nominal $V_{DD}$ of 1.2V and 0.9V, respectively. The gain is ~12dB better with the DDC transistors despite the lower operating voltage.

Fig. 16. Current mirror mismatch comparison for DDC and control process. a) global mismatch for NMOS and PMOS current mirrors and b) local mismatch for NMOS and PMOS current mirrors.