



Corporate Overview

Overview

SuVolta, Inc. develops and licenses semiconductor technologies to significantly reduce integrated circuit (IC) power consumption while maintaining performance.

Reducing power consumption is generally regarded as the biggest challenge in chip design today, a problem which limits the functionality and battery lifetime in portable products including smartphones, tablets and notebooks.

SuVolta has tackled the problem at the heart of electronics systems by addressing the physics of the transistor variation. The SuVolta PowerShrink™ low-power platform significantly lowers power consumption without sacrificing performance across a wide range of ICs, including processors, SRAMs (static-random-access-memory), and SOCs (system-on-a-chips) that are critical to today's mobile systems.

By enabling continued voltage scaling as well as leakage reduction, the SuVolta technology can cut in half the dynamic power consumption of devices as well as reduce leakage power consumption by 5x or more.

Leadership

Bruce McWilliams, PhD – President & CEO (former CEO Tessera, S-Vision, nChip, others)

Scott Thompson, PhD – CTO (former U. Florida, Intel Fellow)

Jeff Lewis – SVP Mktg. and Bus. Development (former Z-RAM, Artisan, other)

Robert Rogenmoser, PhD – SVP, Product Development & Engineering (former IDT, Transmeta, Broadcom, Intel)

Naomi Obinata – Corporate Vice President, Legal and Intellectual Property (former Applied Materials, Intel and TSMC)

Catherine de Villeneuve – Corporate VP Operations (former Tessera, Philips Semiconductors)

Nick Kepler – VP Products (former GLOBALFOUNDRIES, AMD)

Sang-Soo Lee, PhD – VP Analog Design (former Hynix, Pixelplus, LSI Logic, LG Semiconductor)

Pushkar Ranade, PhD – Director Process Development (former Intel)

Lucian Shifren, PhD – Director Device Technology (former Intel)

Board of Directors / Investors

Forest Baskett – NEA
Bill Joy – Kleiner Perkins Caufield & Byers (KPCB)
Bruce McWilliams – SuVolta President & CEO
Dave Orton – CEO, Aptina
Andy Rappaport – August Capital

Product Overview

Progress on controlling power consumption has been impeded by the semiconductor industry's focus on increasing performance. For years, microprocessor performance requirements have driven the industry advancements. With the increase in mobile applications, power has now moved to the forefront as the primary design constraint for digital products. The challenge in the industry is minimizing mobile System on Chip (SOC) power without sacrificing performance or increasing costs and while leveraging existing fab infrastructure, legacy IP and design flows and providing a scalable platform.

SuVolta's PowerShrink™ low-power platform does just that. It is a better planar, bulk CMOS transistor. The SuVolta PowerShrink platform reduces variation and improves performance. It enables circuits and circuit techniques for low voltage and low power operation. It is scalable with existing CMOS fabs processes, design flows and legacy IP. And, it is scalable to advanced geometries.

SuVolta's PowerShrink low-power platform features two key components: SuVolta's Deeply Depleted Channel™ (DDC) CMOS transistor, and SuVolta's DDC-optimized circuits and design techniques to take full advantage of the DDC transistor.

SuVolta's DDC transistor uses a unique channel structure with significant benefits for low power operation compared to conventional transistor technology.

SuVolta's circuits and design techniques take advantage of the unique properties of the DDC transistor to reduce power consumption further by managing threshold voltage (V_T) more effectively than possible with a conventional transistor.

Compatibility is a key aspect of the SuVolta PowerShrink platform. It is compatible with existing fab infrastructure – it doesn't require new equipment or new materials. It is compatible with existing CMOS process integration – with only revision of some existing steps, and no added masks. It is compatible with legacy IP – analog circuits require retuning and logic and memory circuits can migrate with few or no changes. And, it is compatible with existing EDA flows utilizing standard design flows and tools.

SuVolta's PowerShrink low-power platform enables power to be cut in half while performance is maintained.

Platform Advantages

By reducing threshold voltage (V_T) variation by 50 percent, the DDC transistor enables scaling of supply voltage (V_{DD}) by 30 percent (or more) while maintaining the same system clock speed and reducing overall leakage. By improving channel mobility, the DDC transistor increases drive current (I_{eff}) by 10 percent or more. In addition, the DDC transistor supports even more effective threshold voltage management through body biasing enabled by its increased body coefficient.

The SuVolta PowerShrink low-power platform is compatible with current manufacturing and design infrastructure. SuVolta's DDC transistor leverages existing CMOS design rules and process flows, and can be manufactured in existing fabs because it does not require new equipment or new materials. SuVolta's PowerShrink platform also uses conventional design tools and design flows.

Markets

Semiconductor devices technologies for low-power, high-performance, and mid-range applications such as mobile device ICs (processor, baseband, other), memories, FPGAs and networking devices, for fabrication at 65nm and below CMOS process. Advanced mixed-signal designs at a variety of nodes.